AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A component comprising:

a chip having a top surface and having a bottom surface that includes electrically conductive structures;

a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip chip arrangement on the carrier substrate via electrically conductive connections between the electrically conductive structures and the connecting areas;

a support element ~~on~~ at the top surface of the carrier substrate, the support element surrounding the chip ~~carrier substrate~~ but not touching the chip ~~carrier substrate~~; and

a seal that ~~surrounds~~ borders the chip and the support element;

wherein the support element supports the seal.

2. (Previously Presented) The component of claim 1, wherein the electrically conductive connections comprise bumps.

3. (Previously Presented) The component of claim 1, wherein the seal comprises a dielectric layer and substantially covers the top surface of the chip.

4. (Previously Presented) The component of claim 3, wherein the dielectric layer comprises one or more layers.

5. (Currently Amended) ~~A~~ The component of claim 1, wherein the seal comprises ~~comprising~~:

~~a chip having a top surface and having a bottom surface that includes electrically conductive structures;~~

~~a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip-chip arrangement on the carrier substrate via electrically conductive connections between the electrically conductive structures and the connecting areas; and~~

a composite ~~over the top surface of the chip, the composite~~ comprising a dielectric layer and a metal layer, the composite forming a seal with the carrier substrate outside of an area that corresponds to the chip;

wherein the chip has a thickness such that a force resulting from thermal expansion of an electrically conductive connection in a temperature range between -60° C and 85° C is a maximum of 2 Newtons.

6. (Currently Amended) ~~A~~ The component of claim 1, wherein the seal comprises ~~comprising~~:

~~a chip having a top surface and having a bottom surface that includes electrically~~

~~conductive structures;~~

~~a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip-chip arrangement on the carrier substrate via electrically conductive connections between the electrically conductive structures and the connecting areas; and~~

a composite ~~over the top surface of the chip, the composite~~ comprising a dielectric layer and a metal layer above the dielectric layer relative to the top surface of the chip, the composite forming a seal with the carrier substrate outside of an area that corresponds to the chip;

wherein the dielectric layer has a modulus of elasticity of less than 1 Gpa, a thickness of less than 20 μm, or a coefficient of thermal expansion that is greater than $\alpha_{bump}/2$ and that is less than 2 α_{bump}, where α_{bump} is a coefficient of thermal expansion for at least one of the electrically conductive connections.

7. (Currently Amended) ~~A~~ The component of claim 1, wherein ~~comprising:~~

~~a chip having a top surface and having a bottom surface that includes electrically conductive structures;~~

~~a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip-chip arrangement on the carrier substrate via electrically conductive connections between the electrically conductive structures and the connecting areas; and~~

~~a support element on the top surface of the carrier substrate,~~ the support element

~~comprising~~ comprises a shrink frame that substantially encloses the chip.

8. (Previously Presented) The component of claim 7, further comprising a metal layer that substantially covers the top surface of the chip;

wherein the shrink frame forms a seal with the carrier substrate.

9. (Previously Presented) The component of claim 1, 5, 6, or 7, wherein the chip has side surfaces that are sloped so that a cross-section of the chip tapers toward the carrier substrate.

10. (Previously Presented) The component of claim 1, 5, 6, or 7 , wherein the chip has side surfaces that comprise at least one step.

11. (Previously Presented) The component of claim 1, wherein the seal covers edge areas of the chip and the support element; and

wherein the seal does not cover the top surface of the chip.

12. (Previously Presented) The component of claim 1, further comprising a metal layer above the seal relative to the top surface of the chip, the metal layer being on edge areas of the support element and/or on edge areas of the carrier substrate.

13. (Previously Presented) The component of claim 3, wherein the dielectric layer

completely covers the chip and the support element, the dielectric layer forming a seal with the carrier substrate only in areas that do not correspond to the support element so that the chip and the support element are in a shared space that is formed between the dielectric layer and the top surface of the carrier substrate.

14. (Previously Presented) The component of claim 3, wherein the dielectric layer completely covers the top surface of the chip and seals to the support element, the support element comprising a hermetically tight material.

15. (Previously Presented) The component of claim 3, further comprising a metal layer that substantially covers the dielectric layer.

16. (Previously Presented) The component of claim 3, further comprising a filling compound on the dielectric layer.

17. (Previously Presented) The component of claim 16, further comprising a metal layer that forms a seal with the support element outside of an area that corresponds to the chip, or that forms a seal with the carrier substrate outside of an area that corresponds to the support element.

18. (Previously Presented) The component of claim 1 or 7, further comprising a contact metallization on side surfaces of the chip that face the carrier substrate;

wherein the support element comprises a solder frame, the support element being soldered to a contact metallization of the chip.

19. (Previously Presented) The component of claim 18, further comprising a metal layer above a top surface of the chip.

20. (Previously Presented) The component of claim 1, wherein the seal comprises a dielectric material.

21. (Previously Presented) The component of claim 20, wherein the seal comprises at least one of a plastic, an organic plastic, a laminate film, a glass solder and a resin.

22. (Previously Presented) The component of claim 3, wherein the dielectric layer comprises at least one of a plastic, an organic plastic, a laminate film, a glass solder and a resin.

23. (Previously Presented) The component of claim 1, wherein the support element comprises at least one of metal, a ceramic material and plastic.

24. (Previously Presented) The component of claim 1, wherein the support element corresponds to a boundary of an indentation on the carrier substrate.

25. (Previously Presented) The component of claim 1, wherein a height of the support element does not exceed a distance between the top surface of the carrier substrate and a bottom edge of the chip; and

wherein an the inner edge of the support element is under the bottom edge of the chip.

26. (Previously Presented) The component of claim 1, wherein a height of the support element corresponds to, or exceeds, a distance between the top surface of the carrier substrate and a bottom edge of the chip.

27. (Previously Presented) The component of claim 1, 5, 6, or 7, wherein the carrier substrate comprises a low temperature cofired ceramic.

28. (Previously Presented) The component of claim 1, 5, 6, or 7, further comprising surface-mounted-device-capable external contacts on a bottom surface of the carrier substrate.

29. (Previously Presented) The component of claim 1, 5, 6, or 7, wherein the carrier substrate comprises at least two dielectric layers.

30. (Previously Presented) The component of claim 1, 5, 6, or 7, wherein the chip

comprises at least one resonator that works with acoustic surface waves or acoustic volume waves.

31. (Previously Presented) The component of claim 1, 5, 6, or 7, further comprising similar or different chips that are attached to the carrier substrate and that are similarly encapsulated.

32 to 39. (Cancelled)